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# MS-7392

Version: 1.0

## CPU:

Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

## System Chipset:

Intel - MCH (North Bridge) P31  
Intel ICH7R (South Bridge)

## On Board Chipset:

BIOS -- SPI EEPROM  
HD Codec -- ALC888  
LPC Super I/O -- F81182  
LAN-- REALTEK RTL8111C/8111B  
CLOCK -- ICS9LPRS514EGLF

## Main Memory:

DDR II \* 4 (Max 4GB)

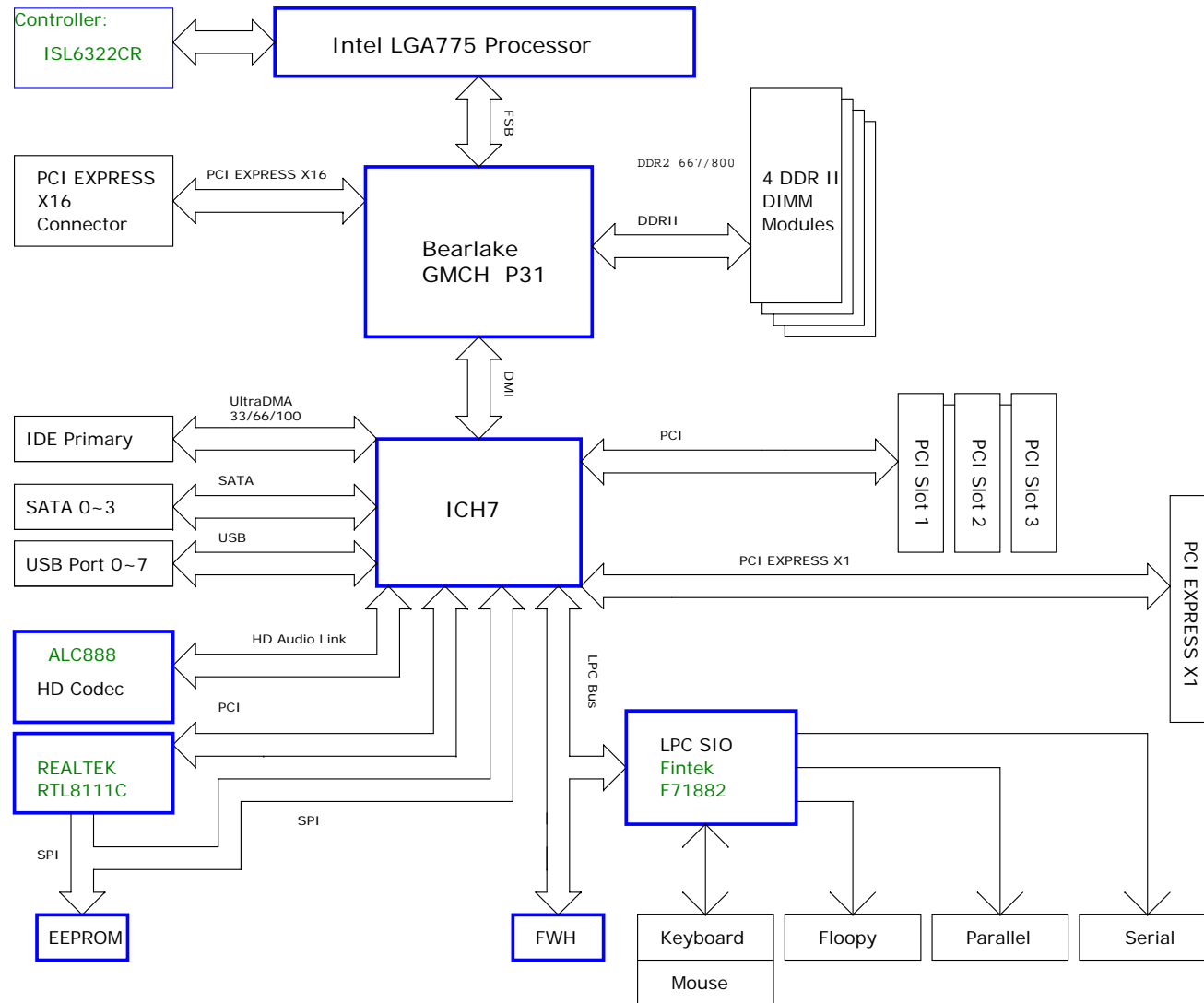
## Expansion Slots:

PCI2.3 SLOT \* 3  
PCI EXPRESS X1 SLOT \* 2  
PCI EXPRESS X16 SLOT

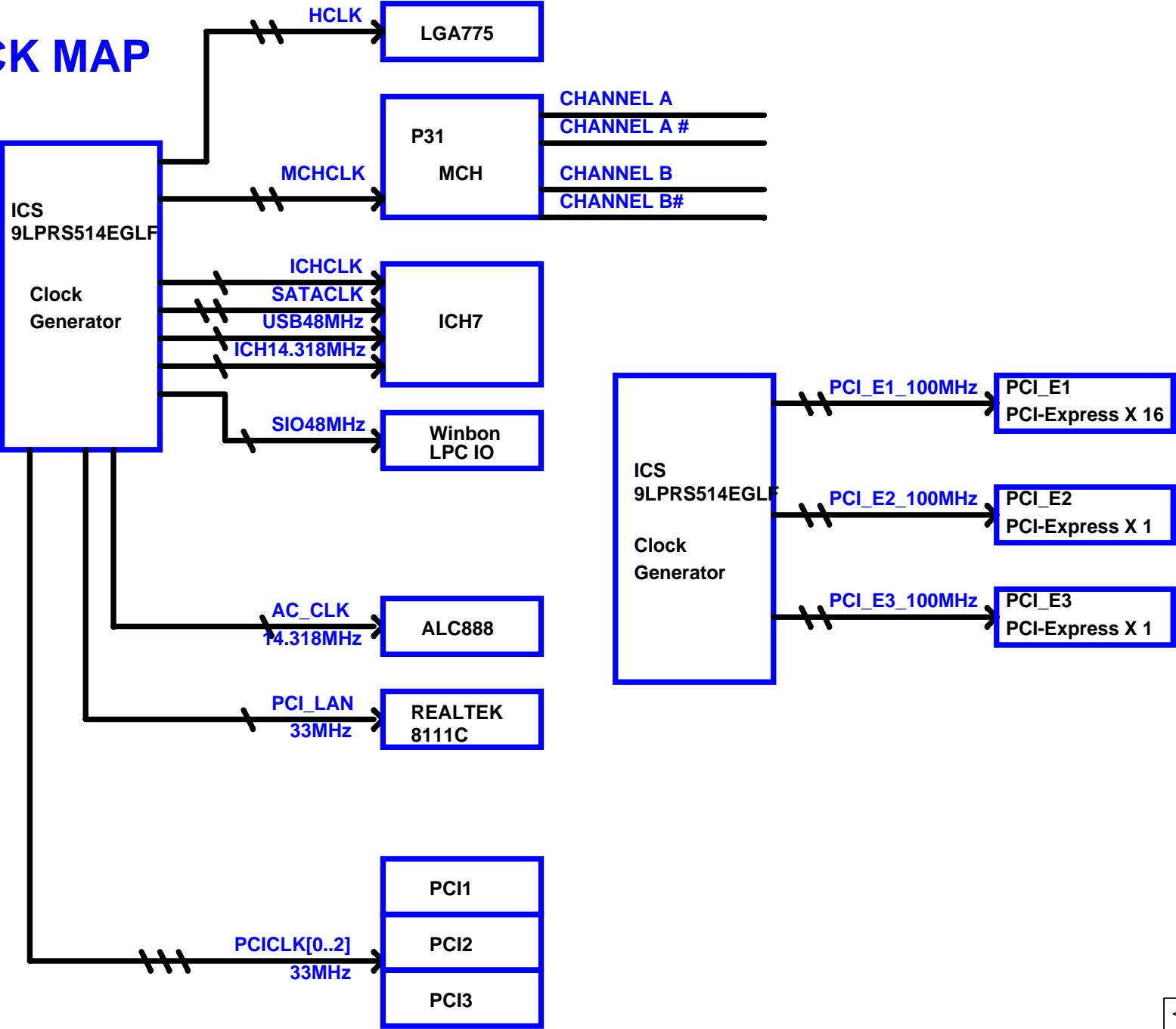
## INTELSIL PWM:

Controller: INTELSIL - ISL6322CR

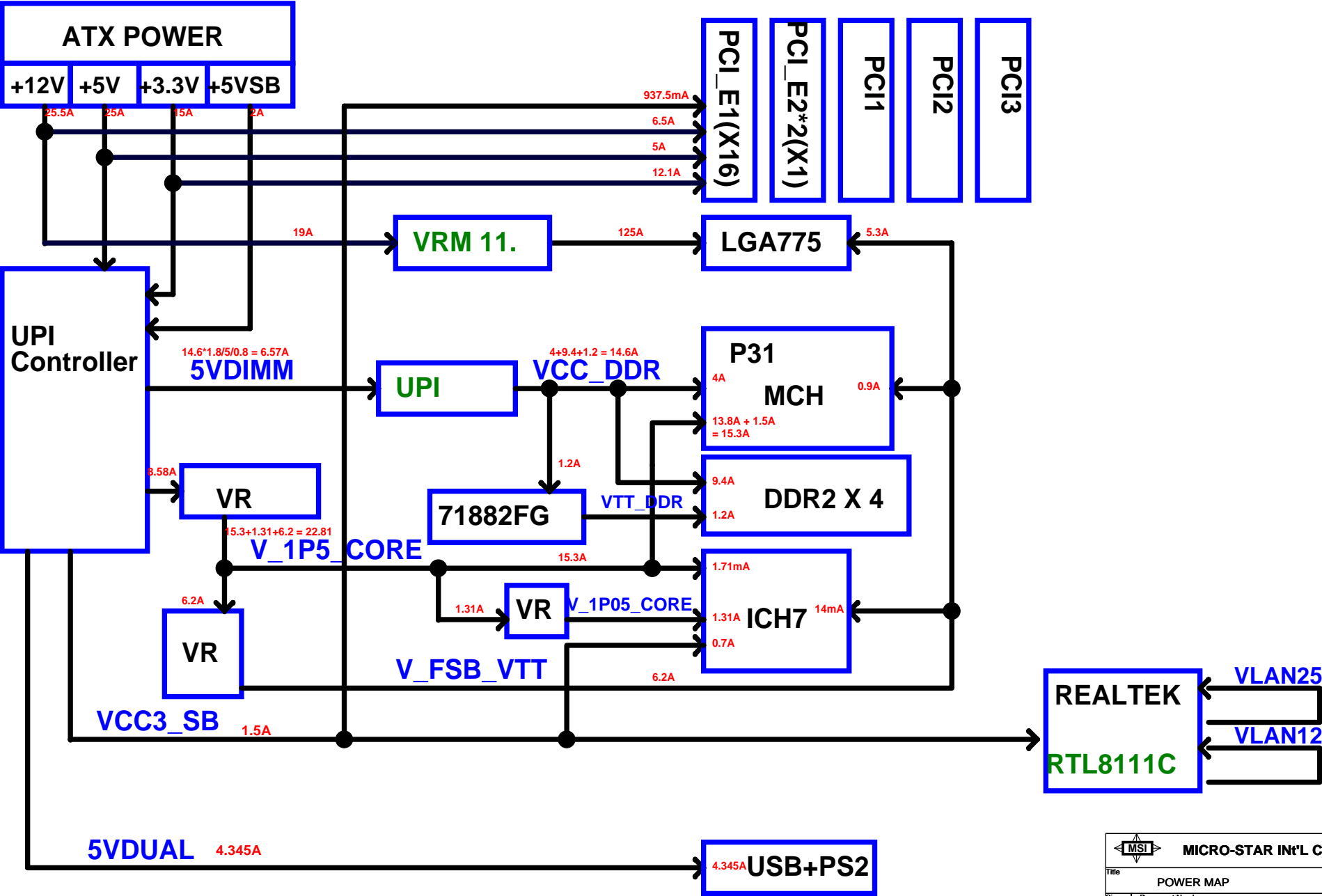
# Block Diagram



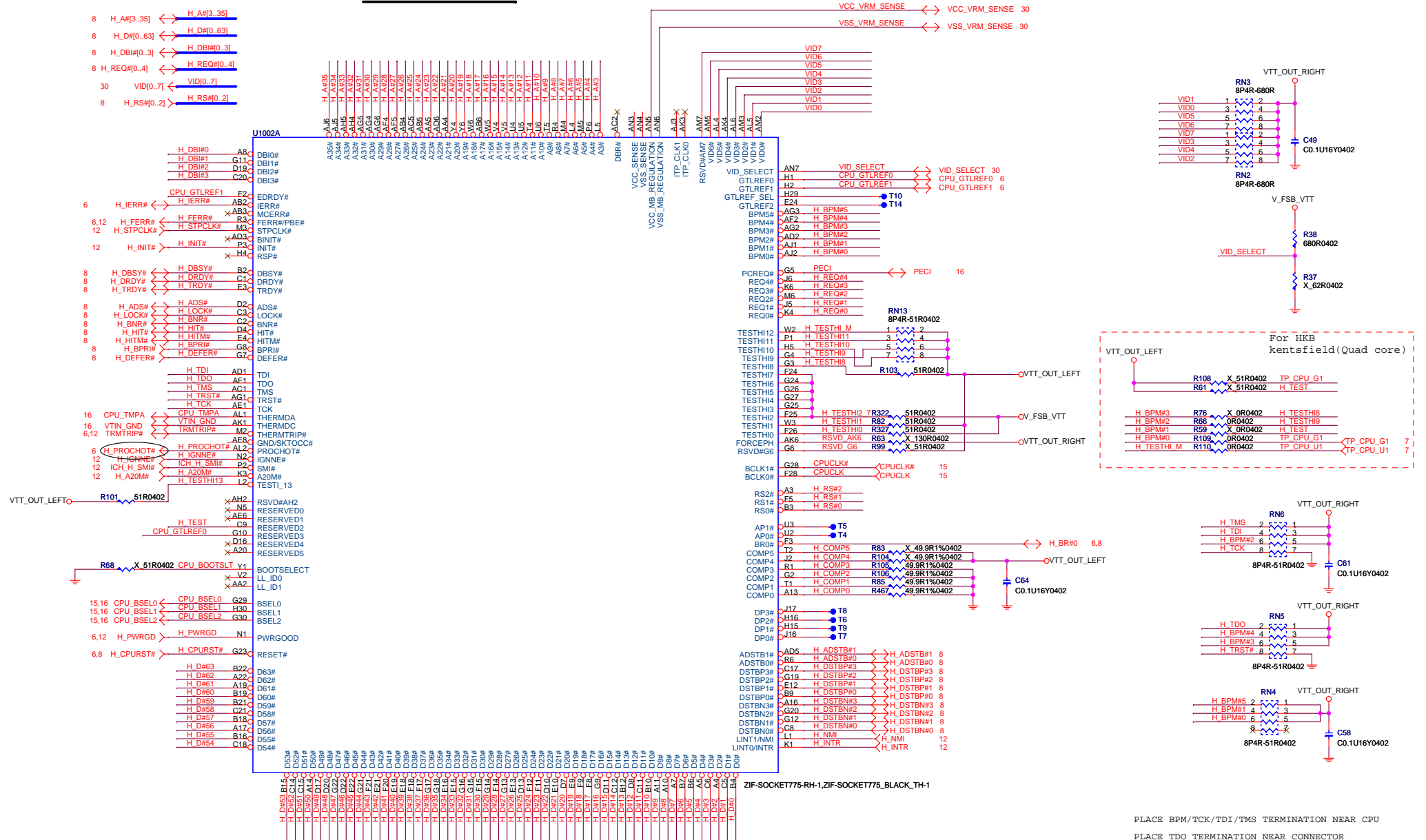
# CLOCK MAP



# POWER MAP



### CPU SIGNAL BLOCK



PLACE BPM/TCK/TDI/TMS TERMINATION NEAR CPU  
PLACE TDO TERMINATION NEAR CONNECTOR



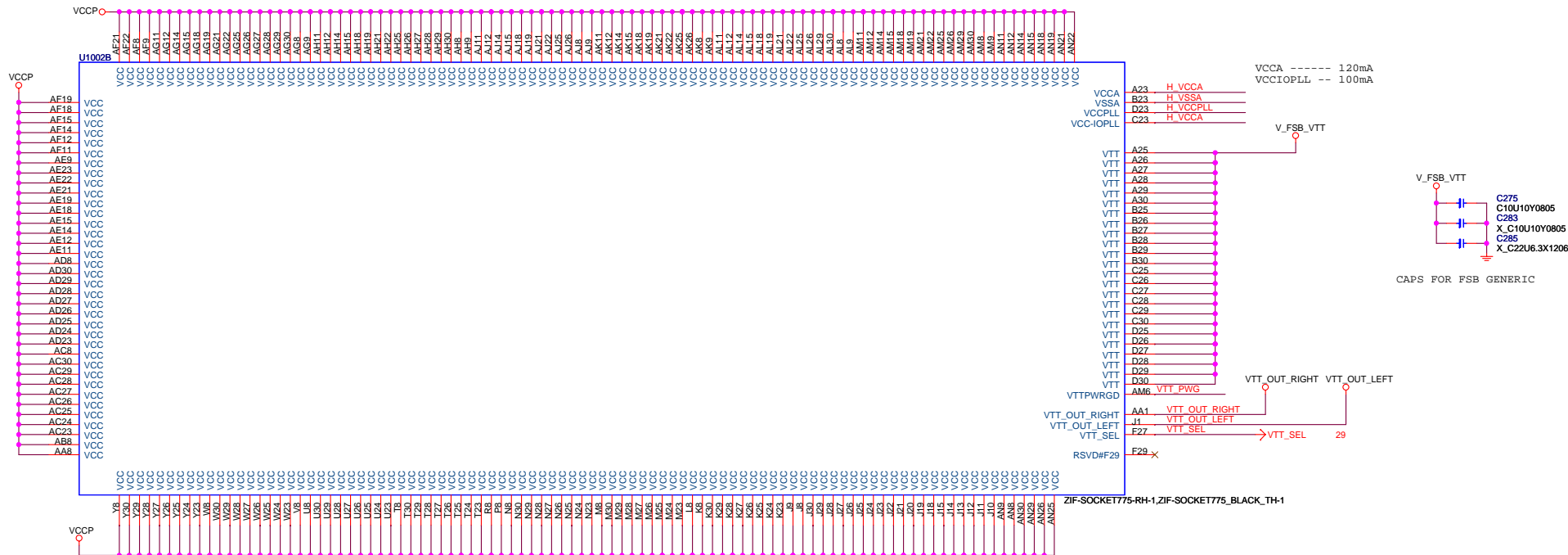
**MICRO-STAR INT'L CO., LTD.**

Title	Intel LGA775 CPU - Signals
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Size	Document Number	Rev
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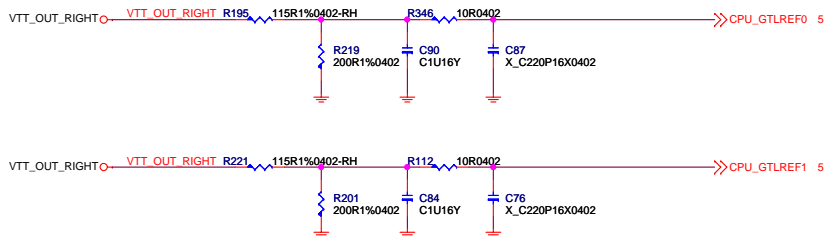
	MS-7392	1.0
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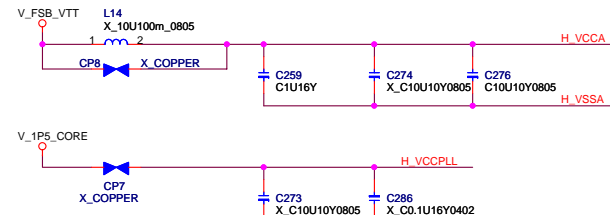


GTLPREF VOLTAGE SHOULD BE 0.635\*VTT

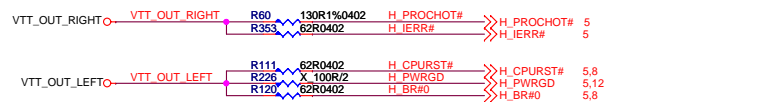
57.6ohm and 100ohm divider



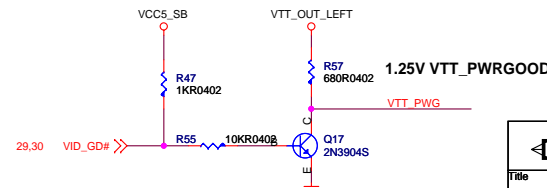
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET  
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS




PLACE AT CPU END OF ROUTE



PLACE AT ICH END OF ROUTE



<b>MICRO-STAR INT'L CO., LTD.</b>		
Title: Intel LGA775 CPU - Power		
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 <b>MICRO-STAR INT'L CO., LTD.</b>	
<b>Title</b> Intel LGA775 CPU - GND	
<b>Size</b>	<b>Document Number</b> MS-7392
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<b>Rev</b> 1.0	

5 H\_A#[3..35] >> H\_A# [3..35]  
5 H\_REQ# [0..4] >> H\_REQ# [0..4]  
5 H\_RS# [0..2] >> H\_RS# [0..2]  
5 H\_D# [0..63] >> H\_D# [0..63]  
5 H\_DB# [0..3] >> H\_DB# [0..3]

H\_A#3 J42 HA3#  
H\_A#4 L39 HA4#  
H\_A#5 L37 HA5#  
H\_A#6 L36 HA6#  
H\_A#7 L36 HA7#  
H\_A#8 K42 HA8#  
H\_A#9 N32 HA9#  
H\_A#10 N34 HA10#  
H\_A#11 M38 HA11#  
H\_A#12 N37 HA12#  
H\_A#13 M36 HA13#  
H\_A#14 R34 HA14#  
H\_A#15 N35 HA15#  
H\_A#16 N38 HA16#  
H\_A#17 U37 HA17#  
H\_A#18 N39 HA18#  
H\_A#19 R47 HA19#  
H\_A#20 P42 HA20#  
H\_A#21 R39 HA21#  
H\_A#22 V36 HA22#  
H\_A#23 R38 HA23#  
H\_A#24 U36 HA24#  
H\_A#25 U33 HA25#  
H\_A#26 R35 HA26#  
H\_A#27 V33 HA27#  
H\_A#28 V35 HA28#  
H\_A#29 V34 HA29#  
H\_A#30 V42 HA30#  
H\_A#31 V38 HA31#  
H\_A#32 Y38 HA32#  
H\_A#33 Y38 HA33#  
H\_A#34 Y39 HA34#  
H\_A#35 AA37 HA35#

5 H\_ADSTB#0 >> M34 HADSTB0#  
5 H\_ADSTB#1 >> U34 HADSTB1#  
H\_REQ#0 F40 HREQ0#  
H\_REQ#1 L38 HREQ1#  
H\_REQ#2 L38 HREQ2#  
H\_REQ#3 G43 HREQ3#  
H\_REQ#4 J37 HREQ4#

5 H\_ADS# >> W40 HADS#  
5 H\_TROY# >> Y40 HTRY#  
5 H\_DRDY# >> W41 HDRDY#  
5 H\_DEFER# >> T43 HDEFER#  
5 H\_HITM# >> Y43 HHITM#  
5 H\_HIT# >> U42 HHIT#  
5 H\_LOCK# >> V41 HLOCK#  
5.6 H\_BR#0 >> AA42 HBREQ0#  
5 H\_BNR# >> W42 HBNR#  
5 H\_BPRI# >> G39 HBPRI#  
5 H\_DBSY# >> U40 HDBSY#

H\_RS#0 U41 HRS0#  
H\_RS#1 AA44 HRS1#  
H\_RS#2 U39 HRS2#

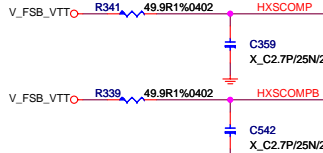
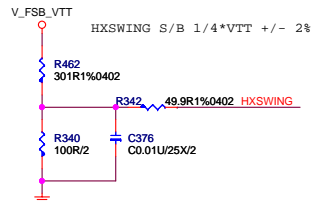
15 CK\_H\_MCH >> R32 HCLKP  
15 CK\_H\_MCH >> U32 HCLKN

10,13,29 CHIP\_PWGD >> AM17 PWROK  
5.6 H\_CPURST# >> C31 HCPURST#

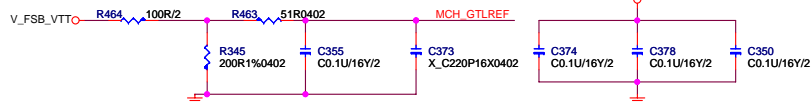
13 ICH\_SYNC# >> R356 ICH\_SYNC#\_R  
10,12,16 PLTRST# >> AM18 PLTRST#  
J13 RSTIN#  
ICH\_SYNC#

HXRCOMP D23 HRCOMP  
HXSCOMP C25 HSCOMP  
HXSCOMP B25 HSWING  
MCH\_GTLREF D24 HDVREF  
B24 HACCVRREF

V\_FSB\_VTT



GTLREF VOLTAGE SHOULD BE 0.67\*VTT=0.804V



HD0# R40 H D#0  
HD1# P41 H D#1  
HD2# R41 H D#2  
HD3# R40 H D#3  
HD4# R42 H D#4  
HD5# M39 H D#5  
HD6# N41 H D#6  
HD7# N42 H D#7  
HD8# L41 H D#8  
HD9# J39 H D#9  
HD10# L42 H D#10  
HD11# J41 H D#11  
HD12# G40 H D#12  
HD13# G40 H D#13  
HD14# F41 H D#14  
HD15# F42 H D#15  
HD16# C42 H D#16  
HD17# D41 H D#17  
HD18# F38 H D#18  
HD19# G37 H D#19  
HD20# E42 H D#20  
HD21# E39 H D#21  
HD22# E37 H D#22  
HD23# C39 H D#23  
HD24# B39 H D#24  
HD25# G33 H D#25  
HD26# F33 H D#26  
HD27# E35 H D#27  
HD28# E35 H D#28  
HD29# H32 H D#29  
HD30# H32 H D#30  
HD31# B34 H D#31  
HD32# J31 H D#32  
HD33# F32 H D#33  
HD34# M31 H D#34  
HD35# E31 H D#35  
HD36# K31 H D#36  
HD37# G31 H D#37  
HD38# K29 H D#38  
HD39# E31 H D#39  
HD40# J29 H D#40  
HD41# F29 H D#41  
HD42# L27 H D#42  
HD43# K27 H D#43  
HD44# H26 H D#44  
HD45# L26 H D#45  
HD46# J26 H D#46  
HD47# M26 H D#47  
HD48# G33 H D#48  
HD49# C35 H D#49  
HD50# E41 H D#50  
HD51# B41 H D#51  
HD52# D42 H D#52  
HD53# C40 H D#53  
HD54# D35 H D#54  
HD55# B40 H D#55  
HD56# C38 H D#56  
HD57# D37 H D#57  
HD58# B33 H D#58  
HD59# D33 H D#59  
HD60# C34 H D#60  
HD61# B35 H D#61  
HD62# A32 H D#62  
HD63# D32 H D#63

HDIN#0# M40 H DB#0  
HDIN#1# J33 H DB#1  
HDIN#2# G29 H DB#2  
HDIN#3# E33 H DB#3


HDSTBP#0 L40 >> H\_DSTBP#0 5  
HDSTBN#0 M43 >> H\_DSTBN#0 5

HDSTBP#1 G35 >> H\_DSTBP#1 5  
HDSTBN#1 H33 >> H\_DSTBN#1 5

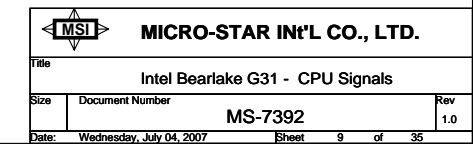
HDSTBP#2 G27 >> H\_DSTBP#2 5  
HDSTBN#2 H27 >> H\_DSTBN#2 5

HDSTBP#3 B38 >> H\_DSTBP#3 5  
HDSTBN#3 D38 >> H\_DSTBN#3 5

Intel-NR880B0V8VA[G31]-A1-RH

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V\_1P25\_CORE

Close to MCH A.S.A.P

R369 5.1KR0402 DMI\_MCH\_IT\_MR\_0\_DP  
R367 5.1KR0402 DMI\_MCH\_IT\_MR\_1\_DP  
R371 5.1KR0402 DMI\_MCH\_IT\_MR\_2\_DP  
R372 5.1KR0402 DMI\_MCH\_IT\_MR\_3\_DP

V\_1P25\_CORE

UTC

22 EXP\_A\_RXP\_0  
22 EXP\_A\_RXN\_0  
22 EXP\_A\_RXP\_1  
22 EXP\_A\_RXN\_1  
22 EXP\_A\_RXP\_2  
22 EXP\_A\_RXN\_2  
22 EXP\_A\_RXP\_3  
22 EXP\_A\_RXN\_3  
22 EXP\_A\_RXP\_4  
22 EXP\_A\_RXN\_4  
22 EXP\_A\_RXP\_5  
22 EXP\_A\_RXN\_5  
22 EXP\_A\_RXP\_6  
22 EXP\_A\_RXN\_6  
22 EXP\_A\_RXP\_7  
22 EXP\_A\_RXN\_7  
22 EXP\_A\_RXP\_8  
22 EXP\_A\_RXN\_8  
22 EXP\_A\_RXP\_9  
22 EXP\_A\_RXN\_9  
22 EXP\_A\_RXP\_10  
22 EXP\_A\_RXN\_10  
22 EXP\_A\_RXP\_11  
22 EXP\_A\_RXN\_11  
22 EXP\_A\_RXP\_12  
22 EXP\_A\_RXN\_12  
22 EXP\_A\_RXP\_13  
22 EXP\_A\_RXN\_13  
22 EXP\_A\_RXP\_14  
22 EXP\_A\_RXN\_14  
22 EXP\_A\_RXP\_15  
22 EXP\_A\_RXN\_15

F15 EXP\_RXP0  
G15 EXP\_RXN0  
K15 EXP\_RXP1  
J15 EXP\_RXN1  
F12 EXP\_RXP2  
E12 EXP\_RXN2  
J12 EXP\_RXP3  
H12 EXP\_RXN3  
J11 EXP\_RXP4  
H11 EXP\_RXN4  
F7 EXP\_RXP5  
E7 EXP\_RXN5  
E8 EXP\_RXP6  
C2 EXP\_RXN6  
D2 EXP\_RXP7  
G8 EXP\_RXP8  
L3 EXP\_RXN8  
L8 EXP\_RXP9  
M8 EXP\_RXP10  
M4 EXP\_RXN10  
L4 EXP\_RXP11  
M5 EXP\_RXP12  
M6 EXP\_RXN12  
R9 EXP\_RXP13  
R10 EXP\_RXN13  
T4 EXP\_RXP14  
R4 EXP\_RXN14  
R6 EXP\_RXP15  
R7 EXP\_RXN15

12 DMI\_MCH\_IT\_MR\_0\_DP  
12 DMI\_MCH\_IT\_MR\_0\_DN  
12 DMI\_MCH\_IT\_MR\_1\_DP  
12 DMI\_MCH\_IT\_MR\_1\_DN  
12 DMI\_MCH\_IT\_MR\_2\_DP  
12 DMI\_MCH\_IT\_MR\_2\_DN  
12 DMI\_MCH\_IT\_MR\_3\_DP  
12 DMI\_MCH\_IT\_MR\_3\_DN

W2 DMI\_RXP0  
V2 DMI\_RXN0  
Y8 DMI\_RXP1  
Y9 DMI\_RXN1  
AA7 DMI\_RXP2  
AA8 DMI\_RXN2  
AA9 DMI\_RXP3  
AA4 DMI\_RXN3

15 CK\_PE\_100M\_MCH  
15 CK\_PE\_100M\_MCH#

B12 GCLKP  
B13 GCLKN

22 SDVO\_CTRL\_DATA  
22 SDVO\_CTRL\_CLK

G17 SDVO\_CTRLDATA  
E17 SDVO\_CTRLCLK

15,16 H\_BSL0  
15,16 H\_BSL1  
15,16 H\_BSL2

G20 BSEL0  
J20 BSEL1  
J18 BSEL2

EXP\_SLR: PCI Express  
Static Lane Reversal  
0: BTX 1: ATX

V\_1P25\_CORE R458 1KR0402 EXP\_SLR  
22 EXP\_PRSNNT\_N R316 0R0402 EXP\_EN

V\_1P25\_CORE R475 X\_0R0402 VCC\_CL\_PLL  
Route solder side  
4milis width

CP28 X\_COPPER

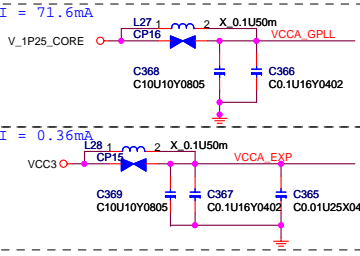
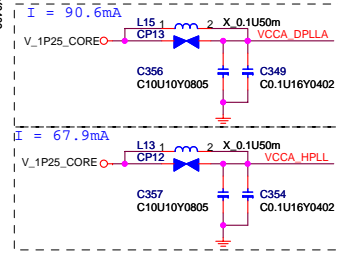
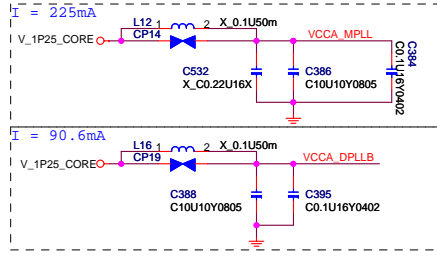
VCC\_A\_HPLL  
VCC\_A\_MPLL  
VCC\_A\_DPLL  
VCC\_A\_DPLLB  
VCC\_A\_GPLL

VCC\_A\_DAC  
VCC\_A\_DAC  
VCC\_A\_EXP  
VCCD\_CRT  
VCCD\_CRT  
VCCD\_CRT  
VSS

VCC3 B17 VCC3\_3

V\_1P25\_CORE

L29 1 2 X 80L4\_30 1206 V\_1P25\_EXP  
CP17 X\_COPPER  
CP18 X\_COPPER



VCCA\_HPLL >> 50mA ; Min Vout >> 1.121V  
VCCA\_MPLL >> 130mA ; Min Vout >> 1.128V  
VCCA\_DPLLA >> 80mA ; Min Vout >> 1.132V  
VCCA\_DPLLB >> 80mA ; Min Vout >> 1.131V  
VCCA\_DAC >> 70mA ; Min Vout >> 3.14V  
VCCD\_CRT >> 20mA ; Min Vout >> 1.425V  
VCCDQ\_CRT >> 0.5mA ; Min Vout >> 1.425V  
VCCA\_EXPPLL >> 50mA ; Min Vout >> 1.129V  
VCC\_SMCLK >> 250mA

BSEL			TABLE
			PSB FREQUENCY
2	1	0	200 MHZ (800)
0	1	0	133 MHZ (533)
0	0	1	

EXP\_TXP0 D11  
EXP\_TXN0 D12  
EXP\_TXP1 B11  
EXP\_TXN1 A10  
EXP\_TXP2 C10  
EXP\_TXN2 D9  
EXP\_TXP3 B9  
EXP\_TXN3 B7  
EXP\_TXP4 D7  
EXP\_TXN4 D6  
EXP\_TXP5 B5  
EXP\_TXN5 B6  
EXP\_TXP6 B3  
EXP\_TXN6 F2  
EXP\_TXP7 E2  
EXP\_TXN7 F4  
EXP\_TXP8 C4  
EXP\_TXN8 J4  
EXP\_TXP9 K3  
EXP\_TXN9 L2  
EXP\_TXP10 K1  
EXP\_TXN10 N2  
EXP\_TXP11 M2  
EXP\_TXN11 P3  
EXP\_TXP12 P3  
EXP\_TXN12 M4  
EXP\_TXP13 S1  
EXP\_TXN13 U2  
EXP\_TXP14 U2  
EXP\_TXN14 T2  
EXP\_TXP15 V3  
EXP\_TXN15 U4

EXP\_A\_TXP\_0 22  
EXP\_A\_TXN\_0 22  
EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
EXP\_A\_TXN\_2 22  
EXP\_A\_TXP\_3 22  
EXP\_A\_TXN\_3 22  
EXP\_A\_TXP\_4 22  
EXP\_A\_TXN\_4 22  
EXP\_A\_TXP\_5 22  
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EXP\_A\_TXN\_11 22  
EXP\_A\_TXP\_12 22  
EXP\_A\_TXN\_12 22  
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EXP\_A\_TXN\_13 22  
EXP\_A\_TXP\_14 22  
EXP\_A\_TXN\_14 22  
EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
K1  
N2  
M2  
P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
EXP\_A\_TXN\_0 22  
EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
EXP\_A\_TXN\_2 22  
EXP\_A\_TXP\_3 22  
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EXP\_A\_TXP\_4 22  
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EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
K1  
N2  
M2  
P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
EXP\_A\_TXN\_0 22  
EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
EXP\_A\_TXN\_2 22  
EXP\_A\_TXP\_3 22  
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EXP\_A\_TXN\_10 22  
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EXP\_A\_TXN\_11 22  
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EXP\_A\_TXN\_12 22  
EXP\_A\_TXP\_13 22  
EXP\_A\_TXN\_13 22  
EXP\_A\_TXP\_14 22  
EXP\_A\_TXN\_14 22  
EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
K1  
N2  
M2  
P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
EXP\_A\_TXN\_0 22  
EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
EXP\_A\_TXN\_2 22  
EXP\_A\_TXP\_3 22  
EXP\_A\_TXN\_3 22  
EXP\_A\_TXP\_4 22  
EXP\_A\_TXN\_4 22  
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EXP\_A\_TXN\_12 22  
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EXP\_A\_TXN\_13 22  
EXP\_A\_TXP\_14 22  
EXP\_A\_TXN\_14 22  
EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
K1  
N2  
M2  
P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
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EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
EXP\_A\_TXN\_2 22  
EXP\_A\_TXP\_3 22  
EXP\_A\_TXN\_3 22  
EXP\_A\_TXP\_4 22  
EXP\_A\_TXN\_4 22  
EXP\_A\_TXP\_5 22  
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EXP\_A\_TXP\_6 22  
EXP\_A\_TXN\_6 22  
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EXP\_A\_TXN\_13 22  
EXP\_A\_TXP\_14 22  
EXP\_A\_TXN\_14 22  
EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
K1  
N2  
M2  
P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
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EXP\_A\_TXP\_12 22  
EXP\_A\_TXN\_12 22  
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EXP\_A\_TXN\_13 22  
EXP\_A\_TXP\_14 22  
EXP\_A\_TXN\_14 22  
EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
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B3  
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E2  
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K3  
L2  
K1  
N2  
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P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
EXP\_A\_TXN\_0 22  
EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
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D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
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U4

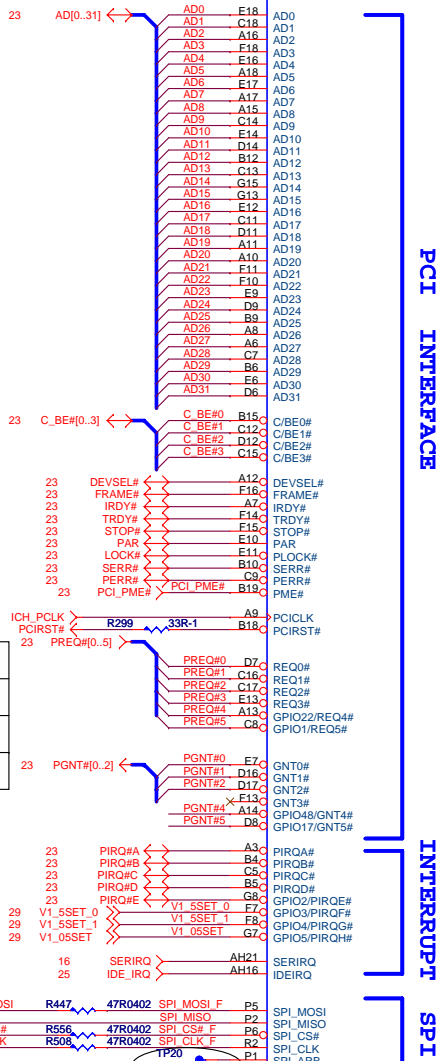
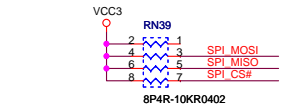
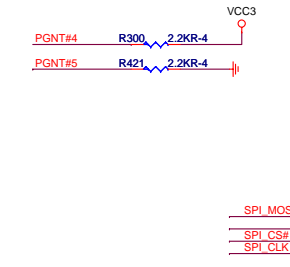
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EXP\_A\_TXN\_0 22  
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EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
EXP\_A\_TXN\_2 22  
EXP\_A\_TXP\_3 22  
EXP\_A\_TXN\_3 22  
EXP\_A\_TXP\_4 22  
EXP\_A\_TXN\_4 22  
EXP\_A\_TXP\_5 22  
EXP\_A\_TXN\_5 22  
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EXP\_A\_TXN\_12 22  
EXP\_A\_TXP\_13 22  
EXP\_A\_TXN\_13 22  
EXP\_A\_TXP\_14 22  
EXP\_A\_TXN\_14 22  
EXP\_A\_TXP\_15 22  
EXP\_A\_TXN\_15 22

D11  
D12  
B11  
A10  
C10  
D9  
B9  
B7  
D7  
D6  
B5  
B6  
B3  
F2  
E2  
F4  
C4  
J4  
K3  
L2  
K1  
N2  
M2  
P3  
P3  
M4  
S1  
U2  
U2  
T2  
V3  
U4

EXP\_A\_TXP\_0 22  
EXP\_A\_TXN\_0 22  
EXP\_A\_TXP\_1 22  
EXP\_A\_TXN\_1 22  
EXP\_A\_TXP\_2 22  
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EXP\_A\_TXN\_15 22

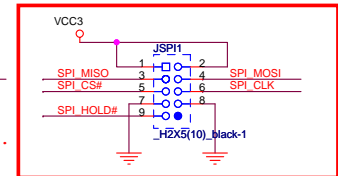
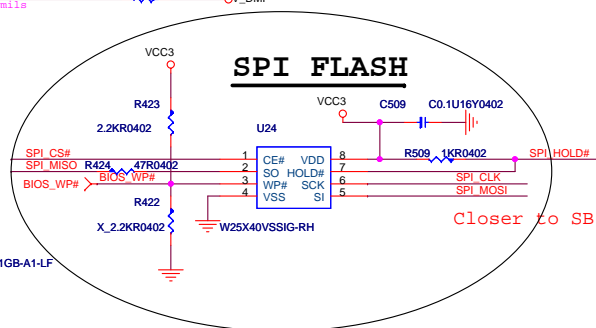
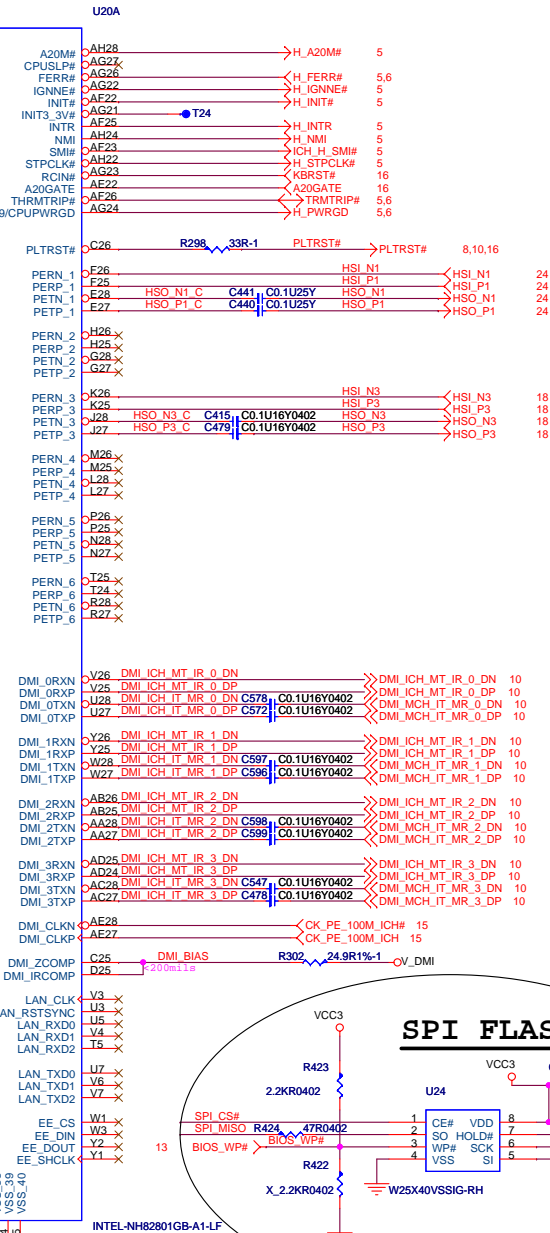


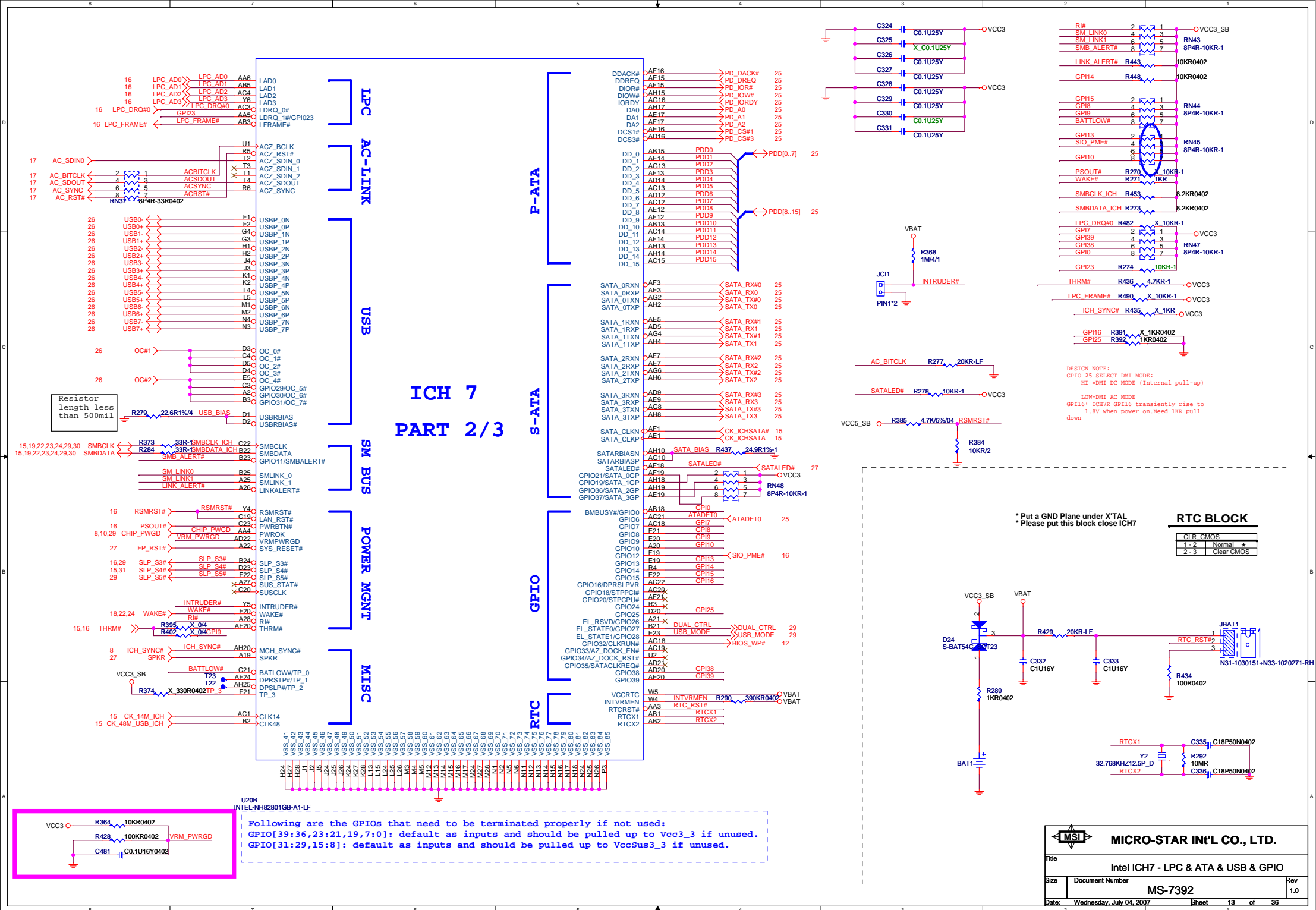
GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC



## ICH 7 PART 1/3

CPU  
PCI  
PCI EXPRESS  
DIRECT MEDIA  
LAN  
INTERRUPT  
SPI

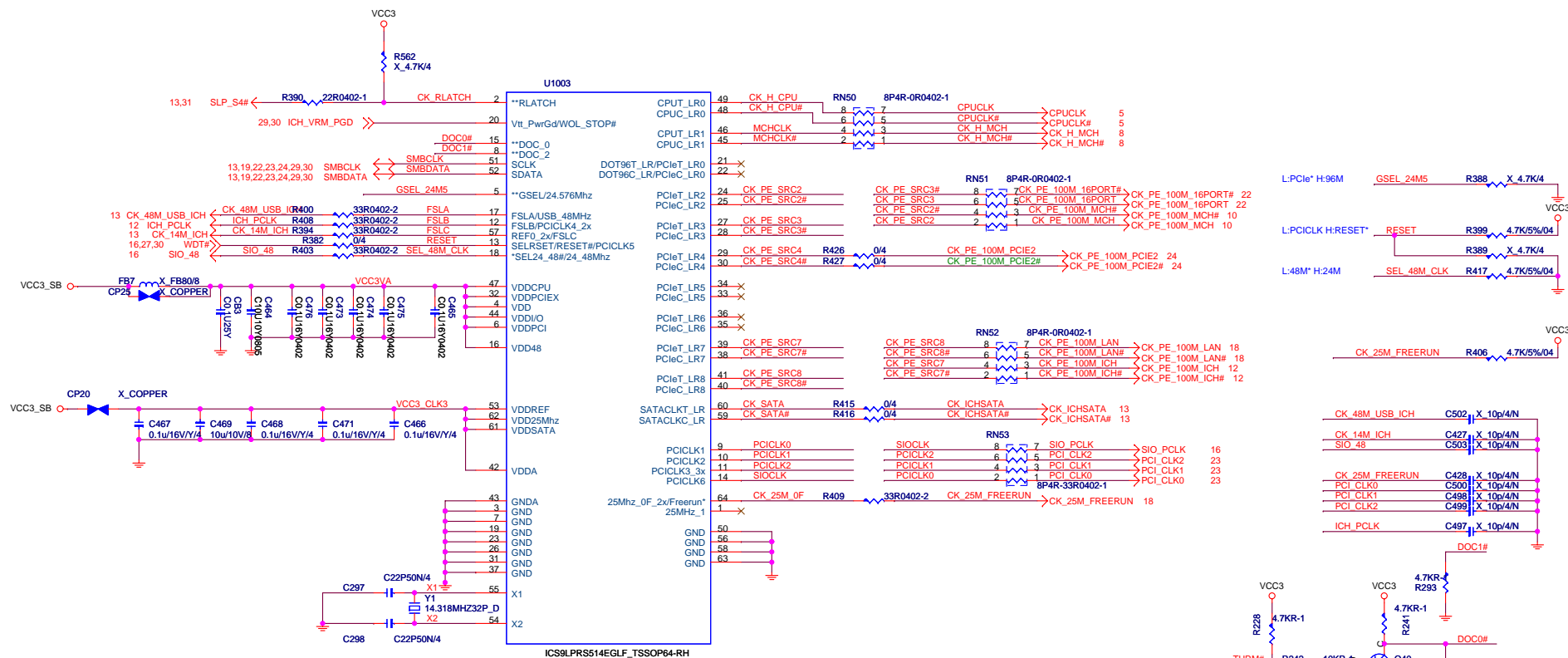




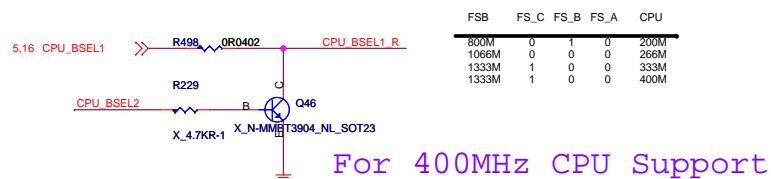
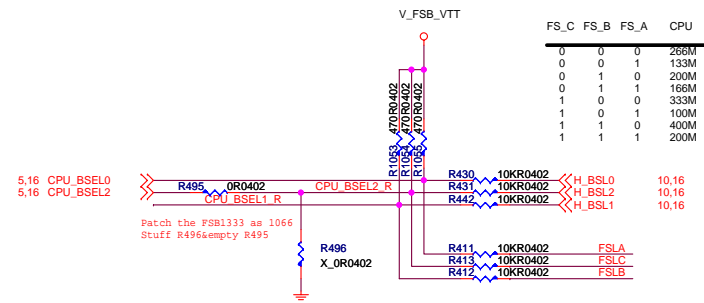




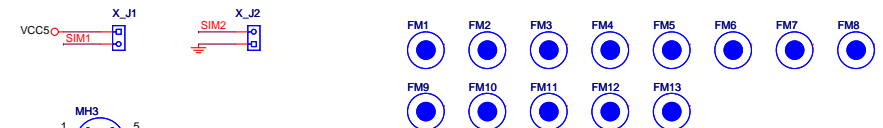
## Clock Generator - ICS9LPRS514EGLF



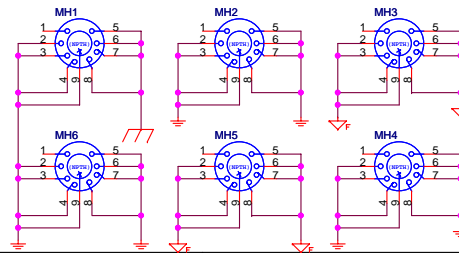
### CPU Frequency Selection

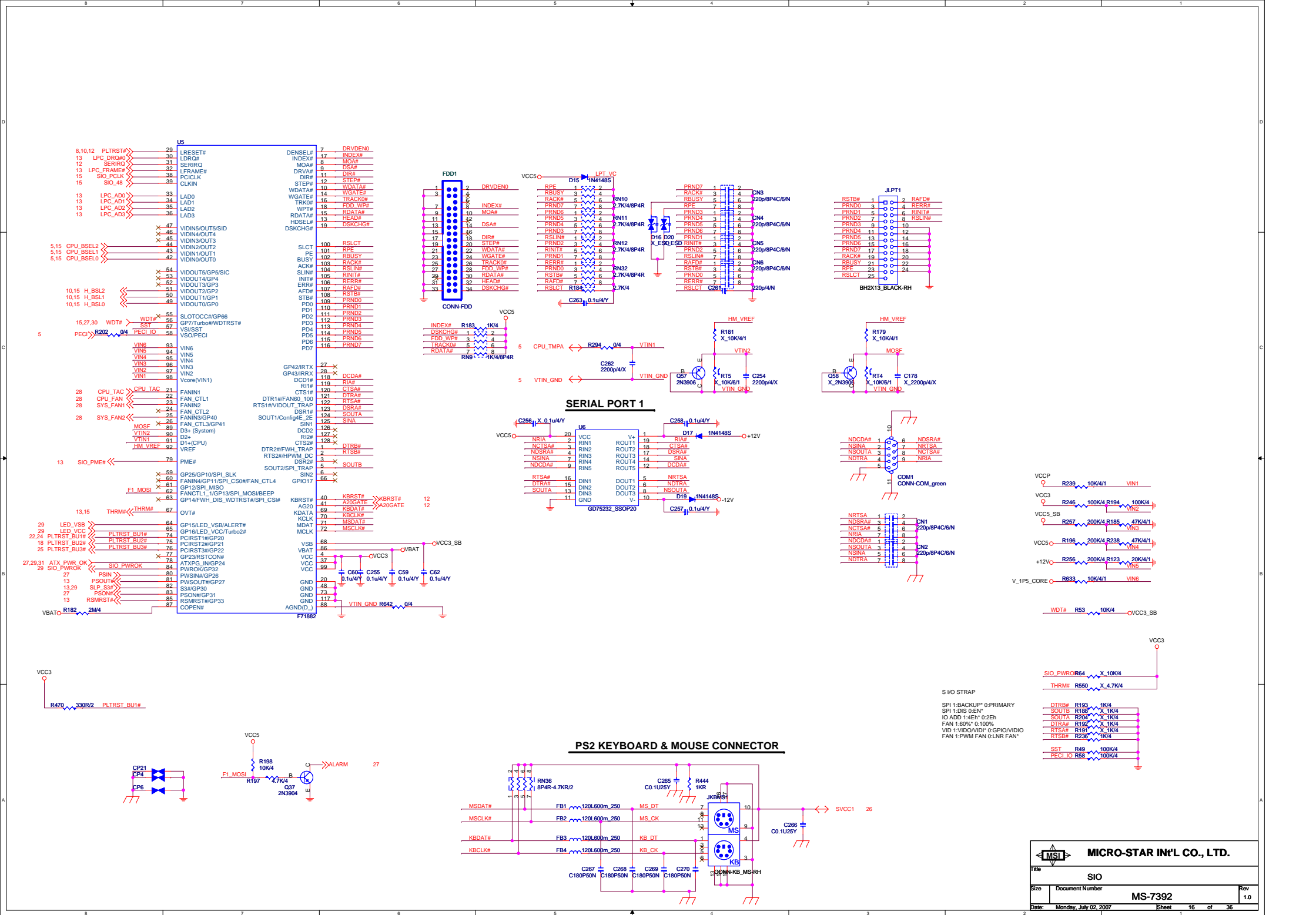


### Optics Orientation Holes



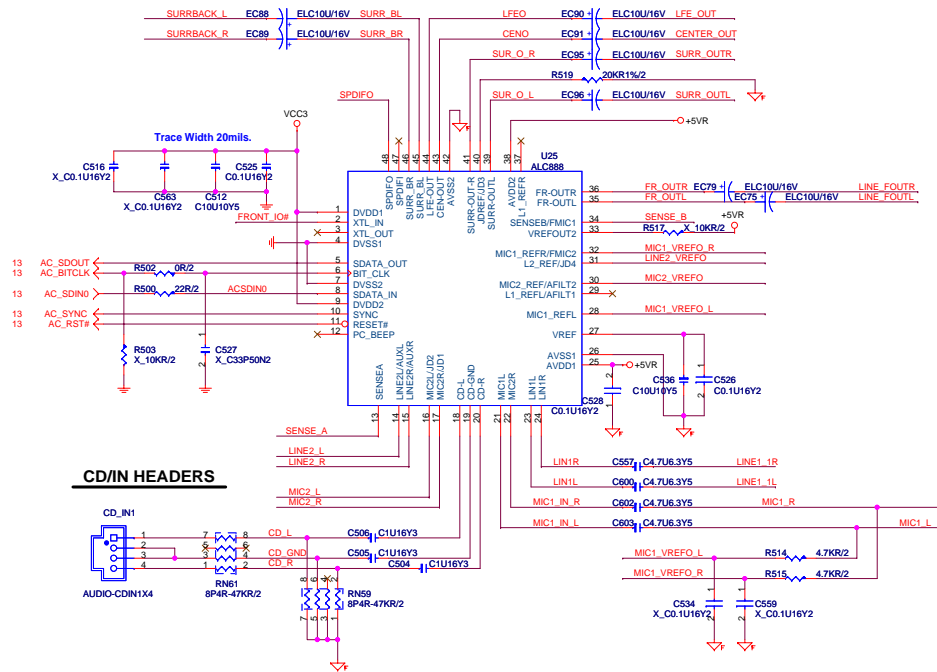
### Mounting Holes



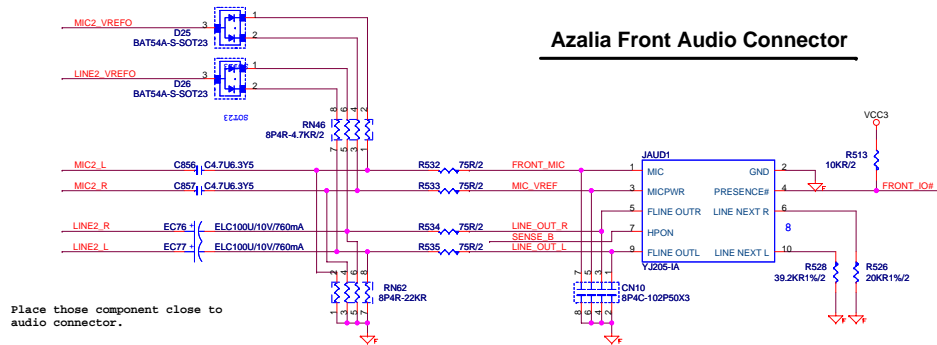




## ALC888 CODEC

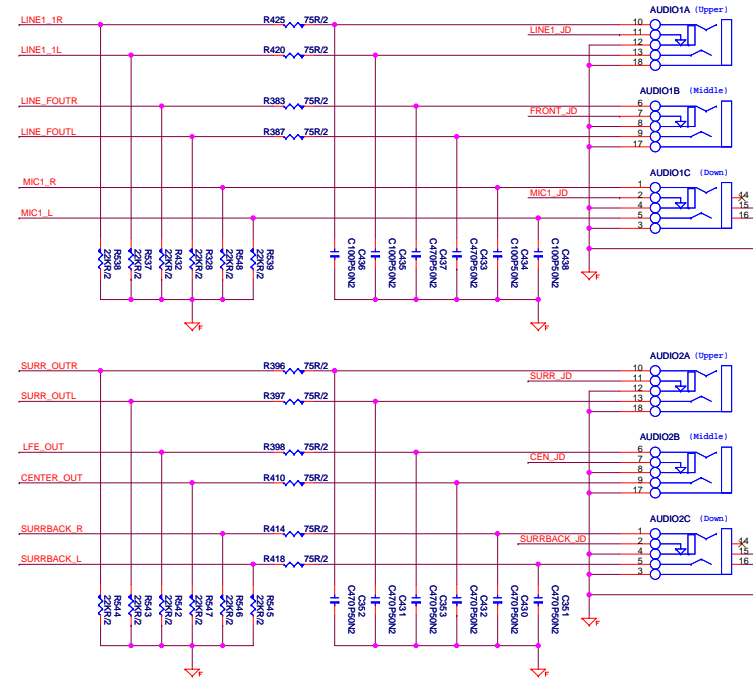


## Azalia Front Audio Connector

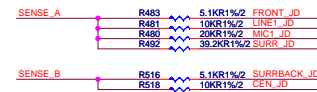


Place those component close to  
audio connector.

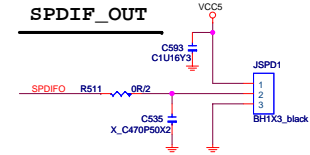
ALC888 JACK



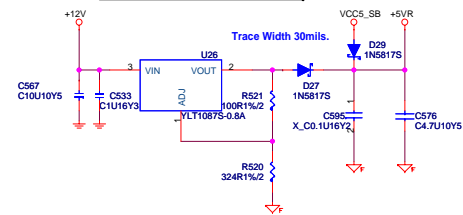
ALC888 JACK DETECT



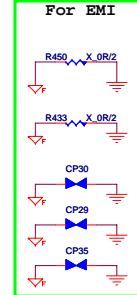
## SPDIF\_OUT



### AUDIO CODE REGULATORS

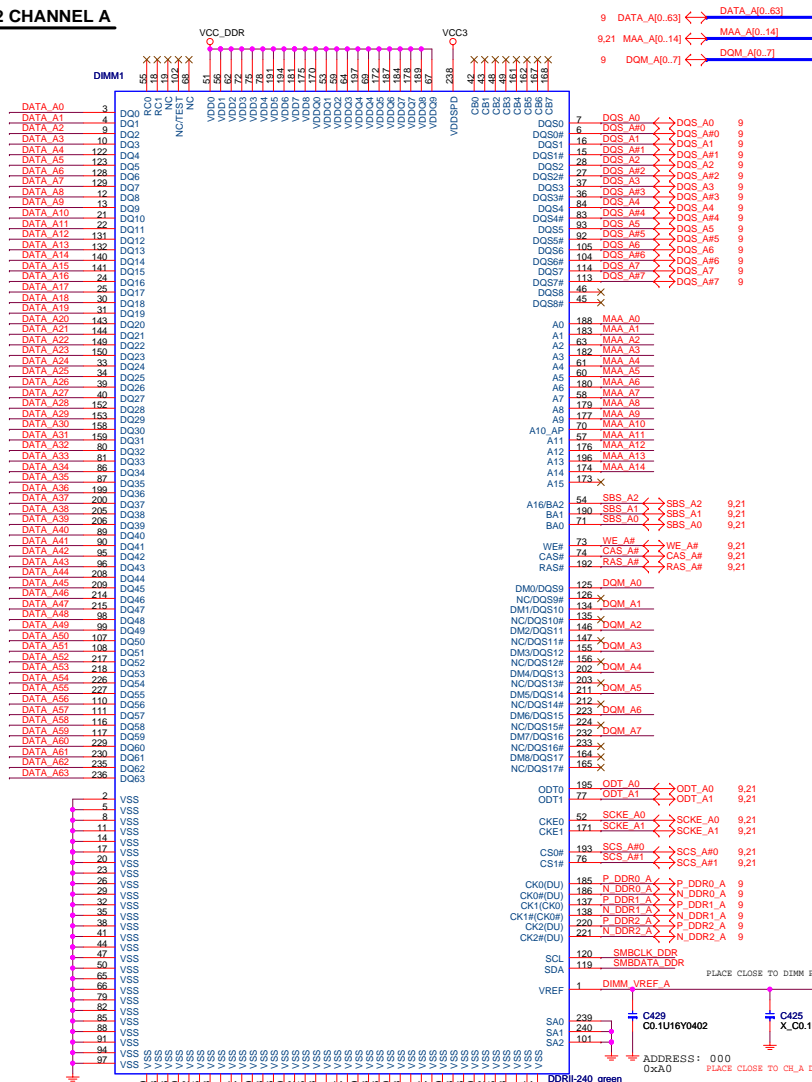


For EMI



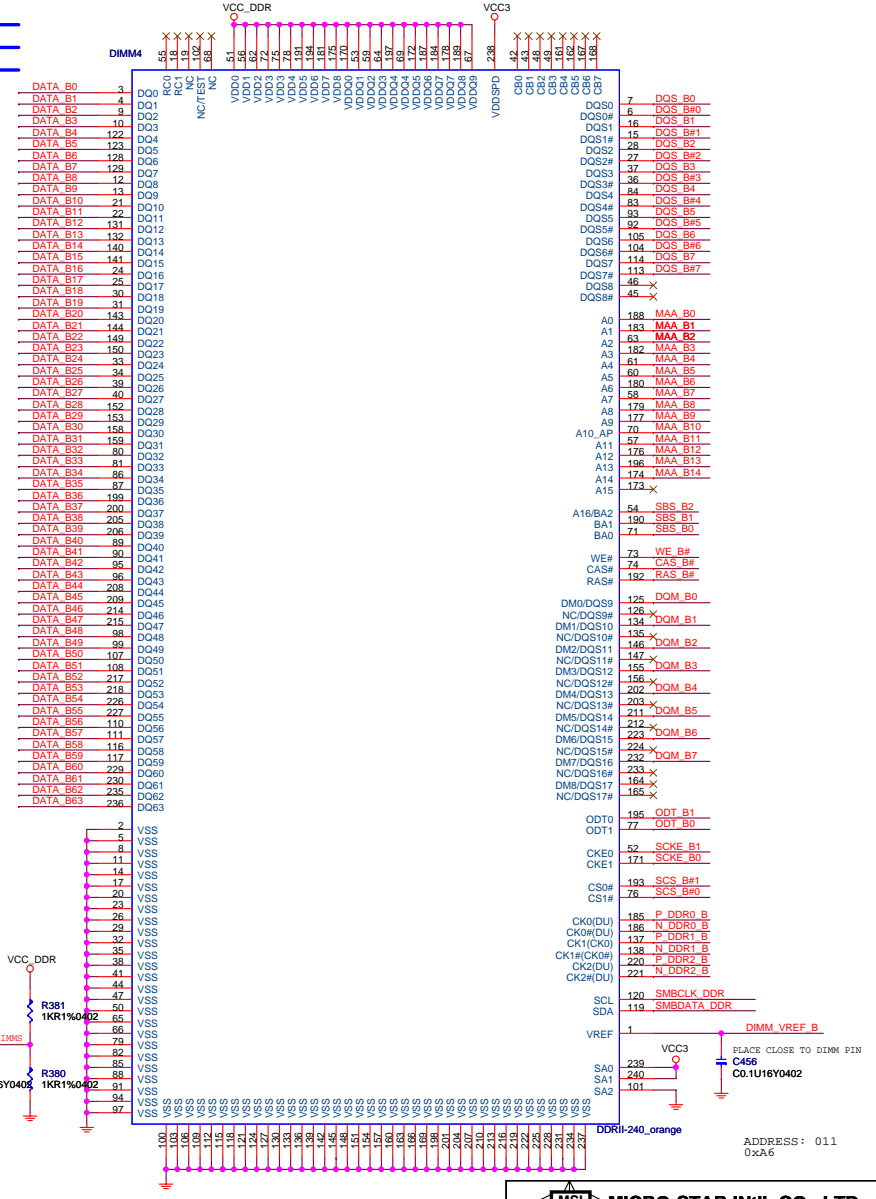


# DDR2 CHANNEL A

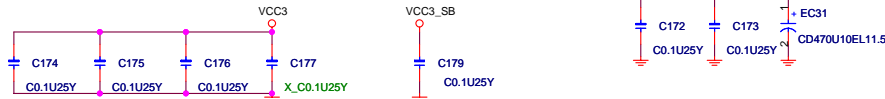


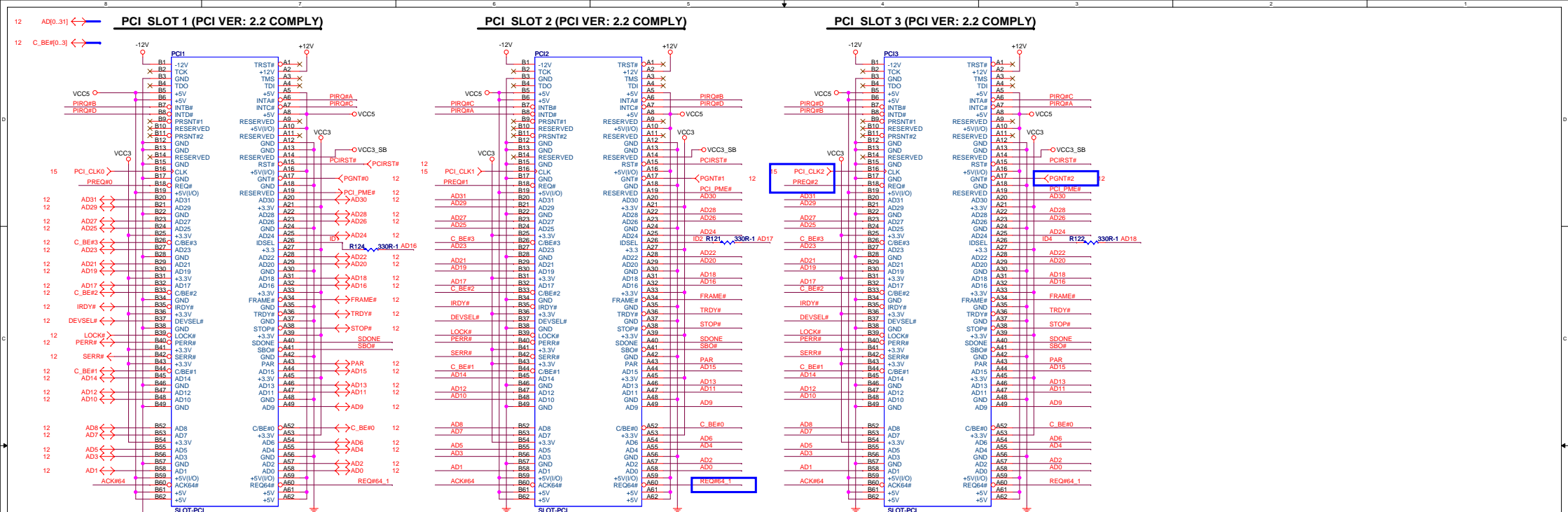
13,15,22,23,24,29,30 SMBCLK  
13,15,22,23,24,29,30 SMBDATA

# DDR2 CHANNEL B









IDSEL = AD16

MASTER = PREQ#0

PIRQ#A

IDSEL = AD17

MASTER = PREQ#1

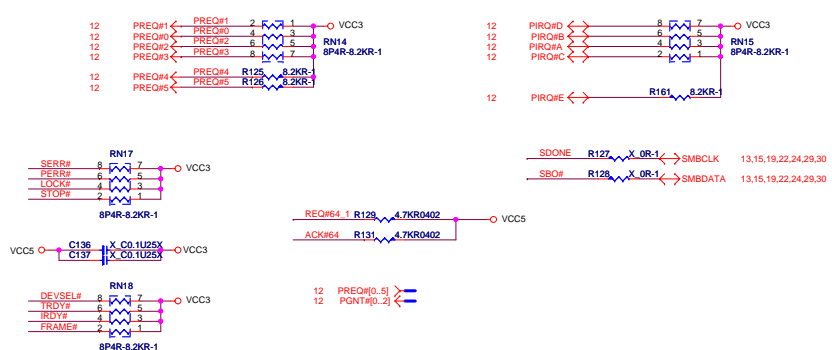
PIRQ#B

IDSEL = AD18

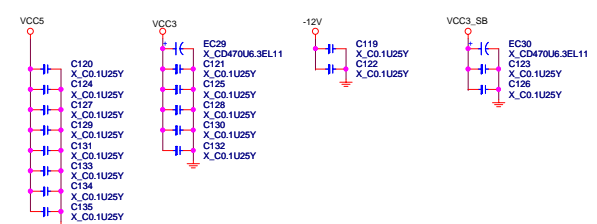
MASTER = PREQ#2

PIRQ#C

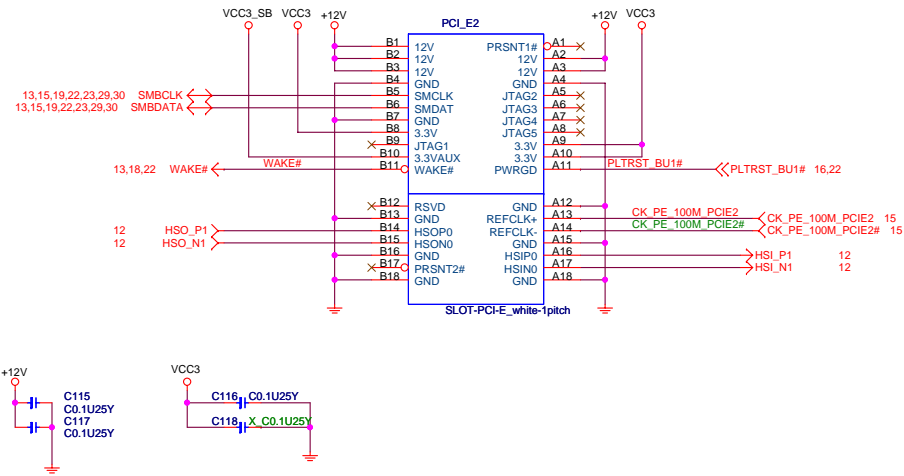
### PCI PULL-UP / DOWN RESISTORS



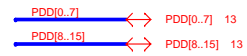
### PCI SLOT DECOUPLING CAPACITORS



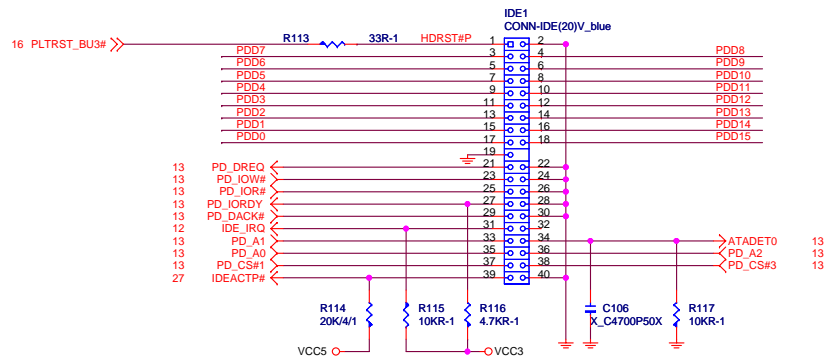
# PCI EXPRESS 1-PORT



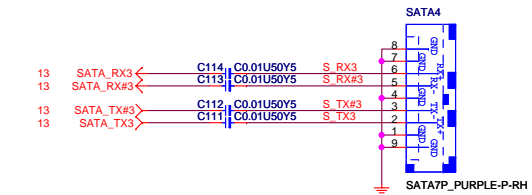
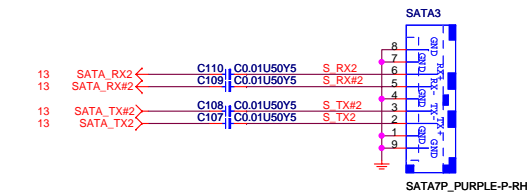
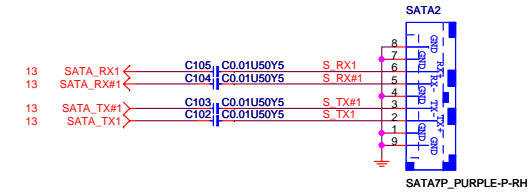
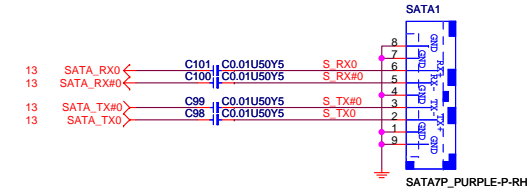




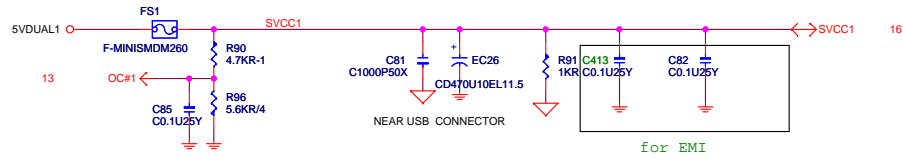
### ATA 33/66/100 IDE Connectors



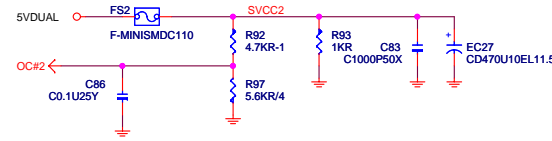
### SERIAL ATA CONNECTOR BLOCK



## POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



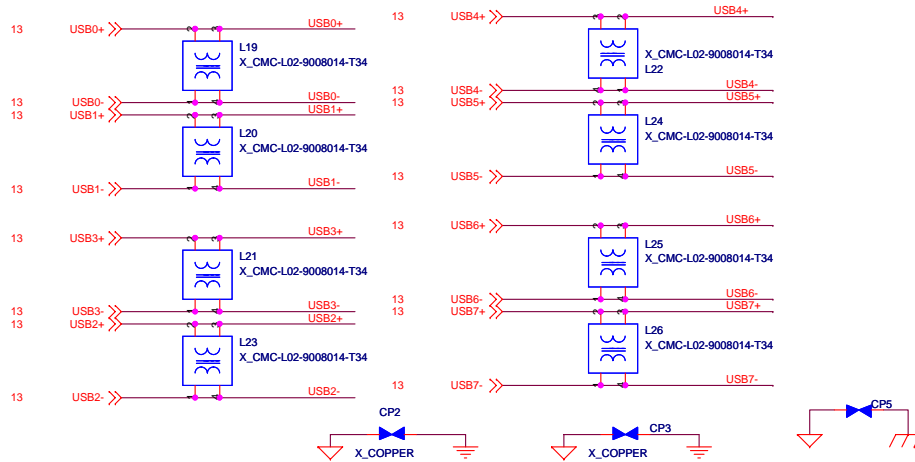
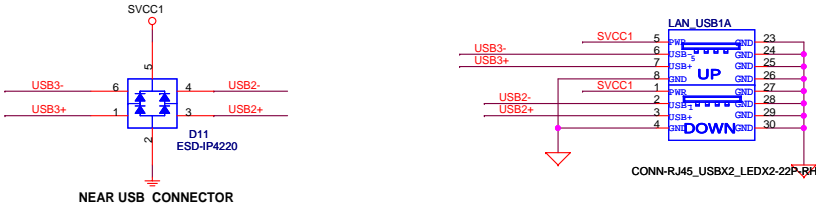
## POWER CIRCUIT FOR USB PORT (FRONT)



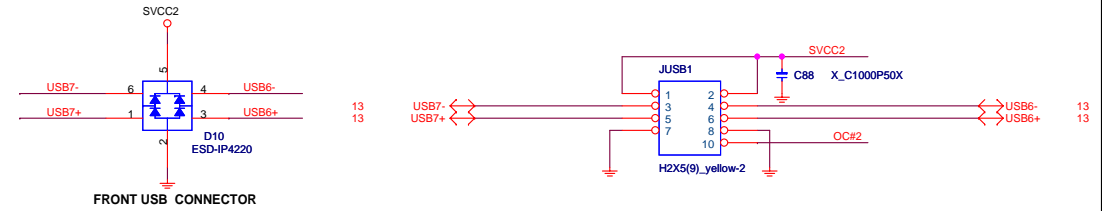
## REAR PANEL USB CONNECTOR FOR USB PORT 0,1



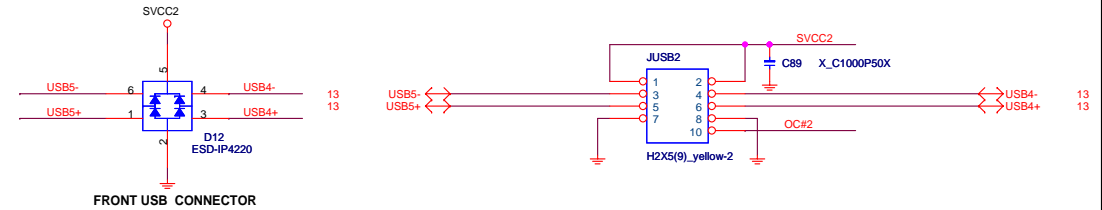
## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

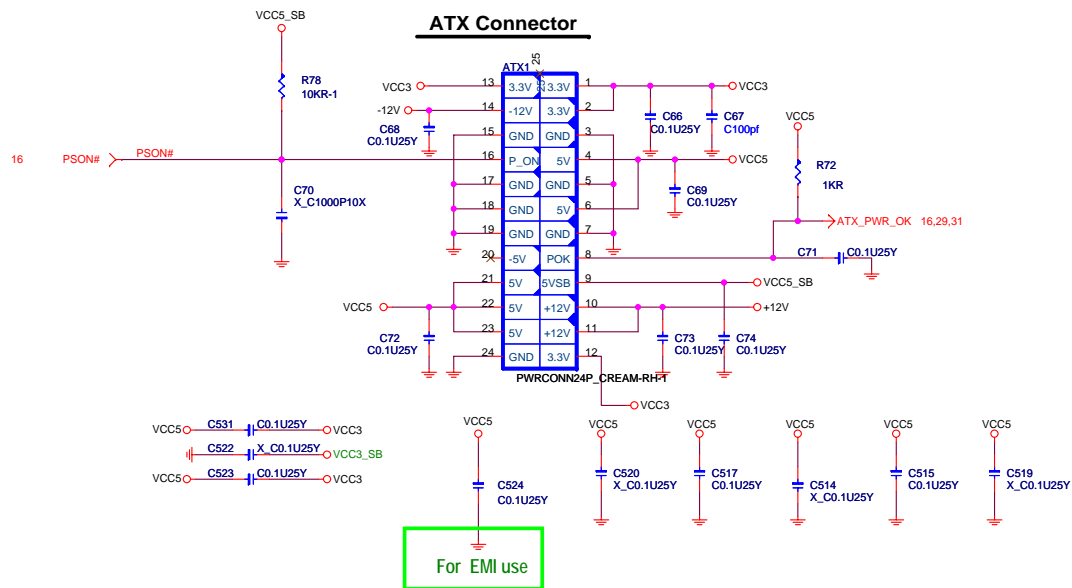


## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

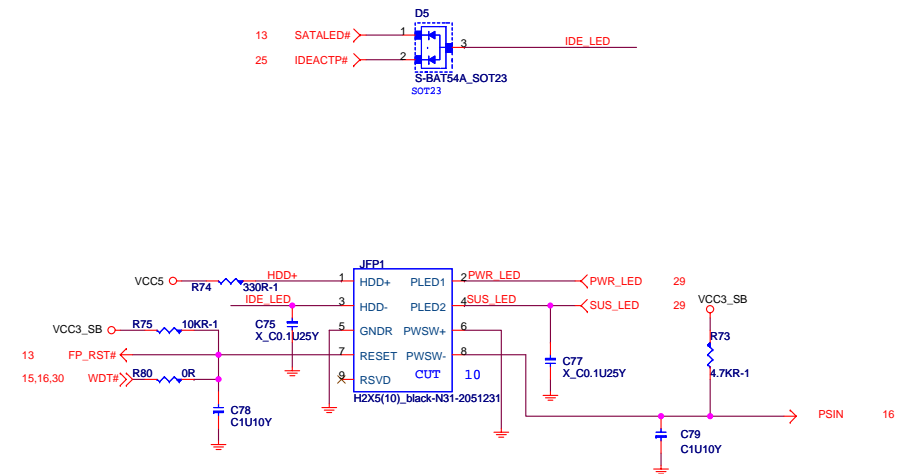


## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

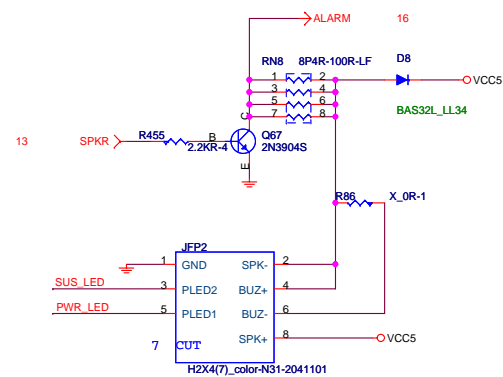




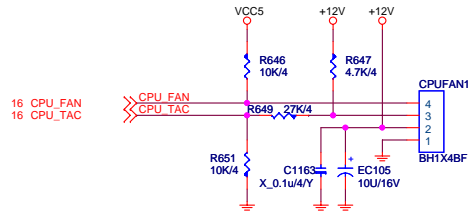
### INTEL/PB Front Panel Connector



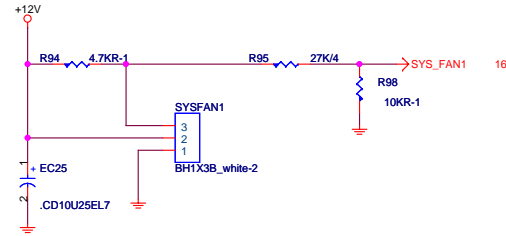
### MSI Front Panel Connector



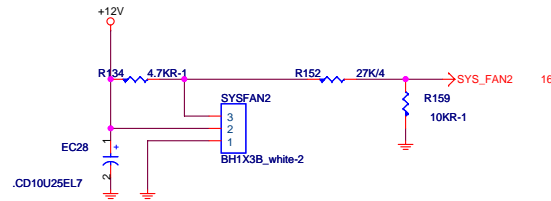
## CPU FAN



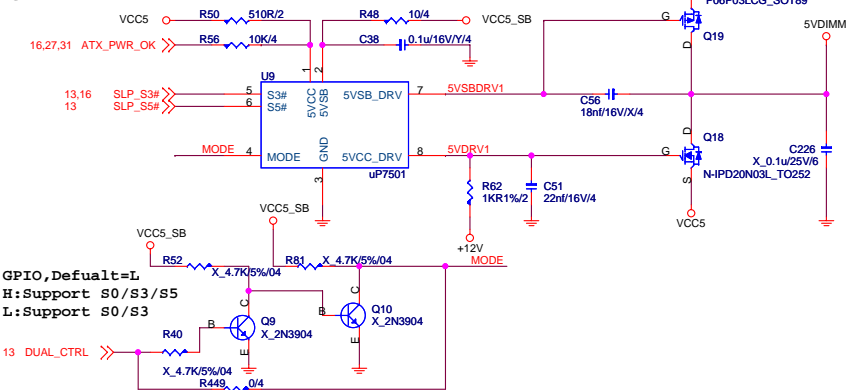
## SYSTEM FAN1



## SYSTEM FAN2

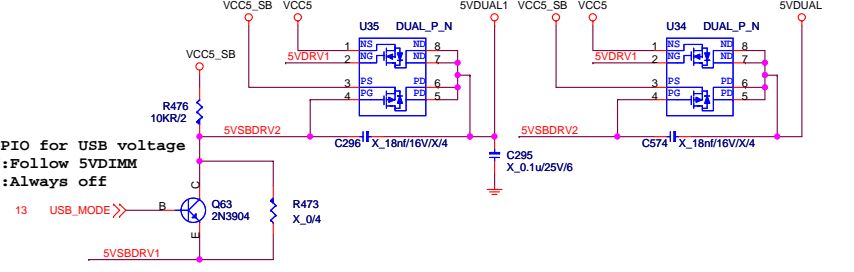


5VDIMM FOR DDR



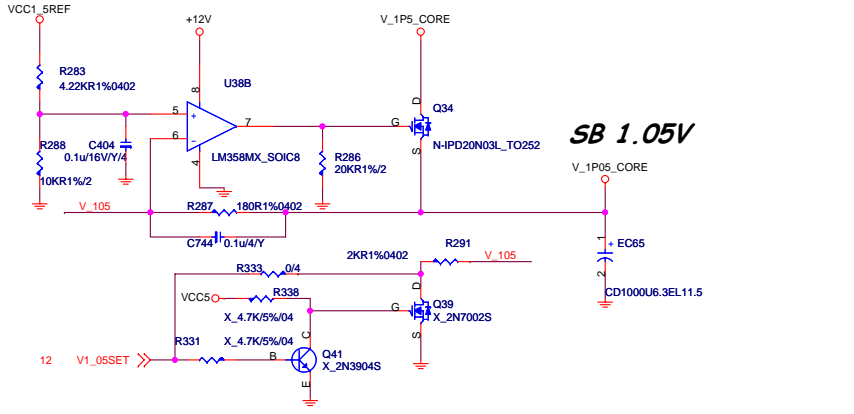
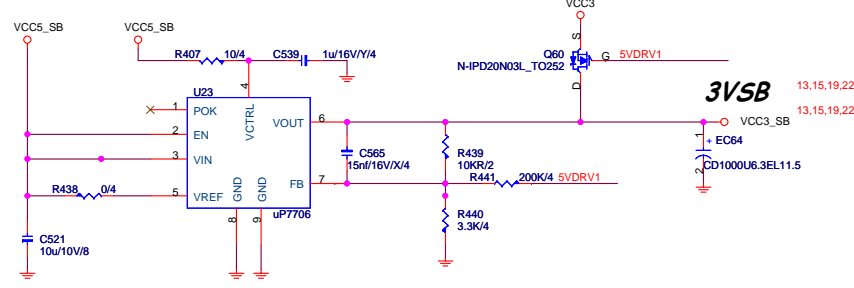
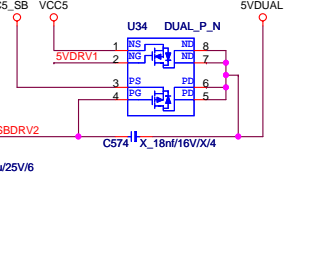
GPIO, Default=L  
H: Support S0/S3/S5  
L: Support S0/S3

5VSB FOR Rear USB



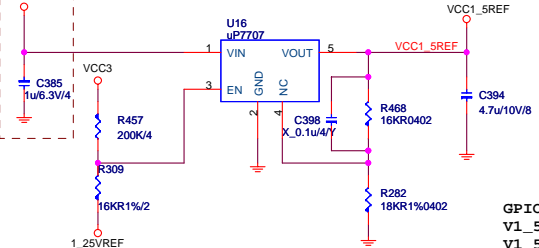
GPIO for USB voltage  
H: Follow 5VDIMM  
L: Always off

5VSB FOR Front USB

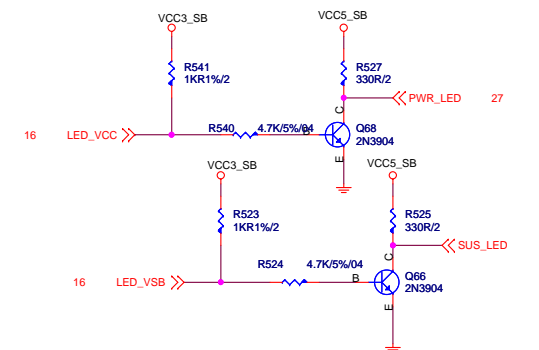


SB 1.05V

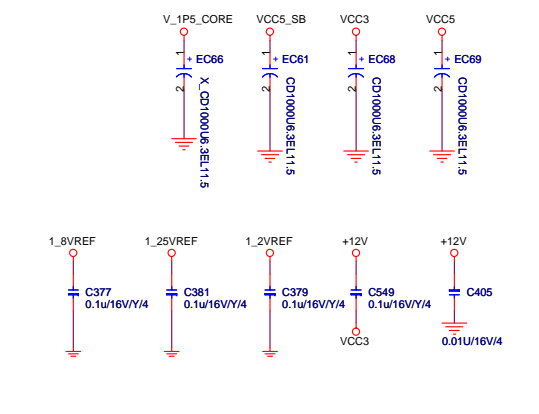
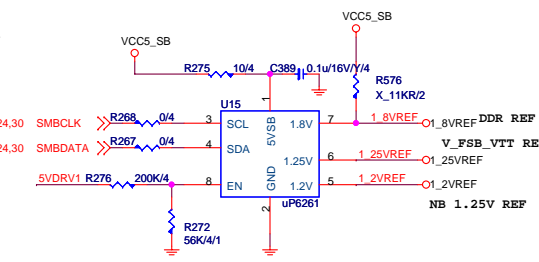
VCC1\_5REF



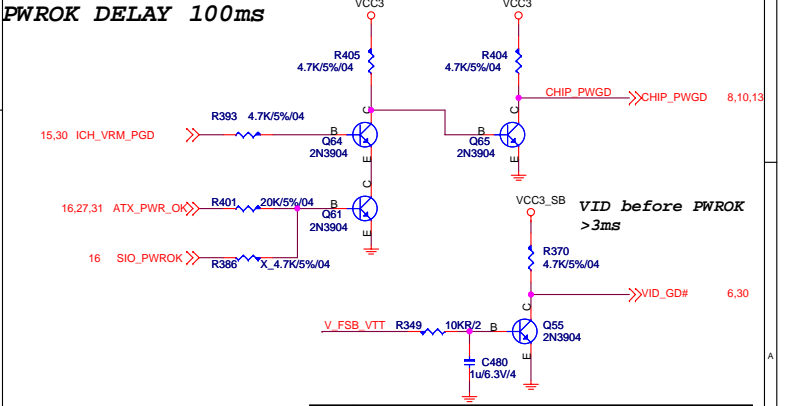
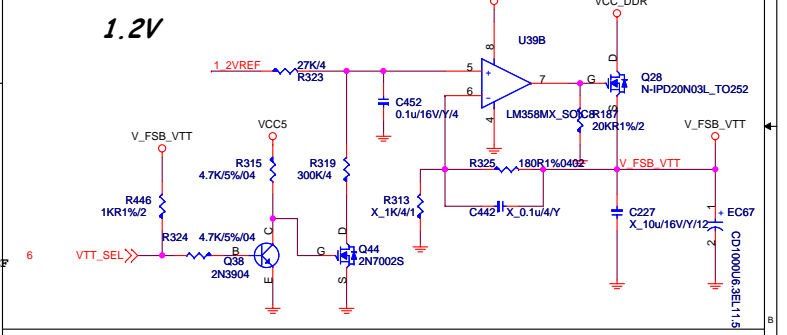
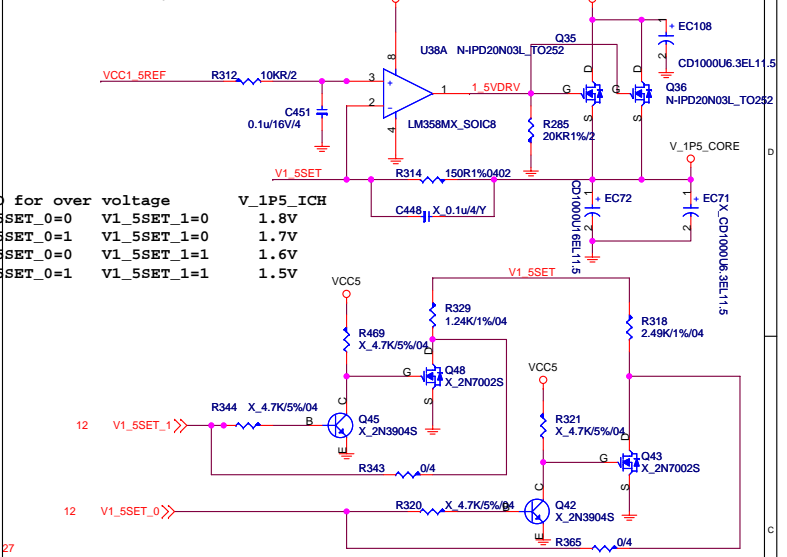
LED ( for Fintek 71882)

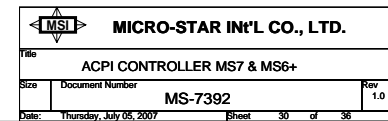


reference Voltage



SB 1.5V





[illegible]

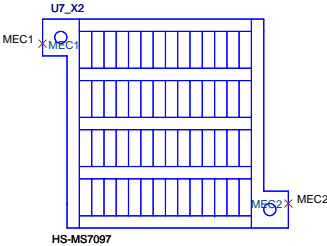
Auto-BOM Manual Parts

PCB1  
PCB  
PCB-7392

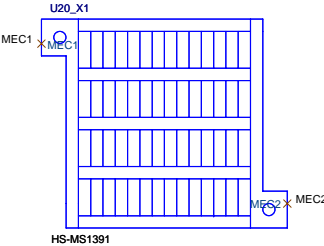
BATTERY1  
BATTERY-CR2032

Auto-BOM Option Parts

P31 HEATSINK



ICH7 HEATSINK





1. Modify VCCA\_EXP pullup VCC3 (page 10);
2. Modify USB 5vdual N-MOS to P-MOS (page 29);
3. Modify ICH7 VRM\_PWRGD sequence (page 13);
4. Change LAN to RTL8111C CO-LAY RTL8111B (page 18);
5. Add EC28 FOR SYSTEM FAN2 (page 28);
6. Change PCI-SLOT pull up power VCC5 to VCC3 (page 23);

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Title <Title>			
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